



Z16C01/C02

CPU CENTRAL PROCESSING UNIT

FEATURES

| Part | Memory Address | Memory Extension | Speed (MHz) |
|--------|----------------|------------------|-------------|
| Z16C01 | 8 Mbytes | 48 Mbytes | 10 |
| Z16C02 | 64 Kbytes | 384 Kbytes | 10 |

- 40/48-Pin PDIP and 44-Pin PLCC Packages
- $+4.5 \leq V_{CC} \leq +5.5$ -Volt Operating Range
- Low-Power CMOS
- 0°C to +70°C Temperature Range

- Extendable Register Files
- Nine Basic Instruction Types
- Eight User-Selectable Addressing Modes
- Seven Data Types
- Supports Three Interrupt Types and Four Traps
- RISC-Like Load/Store Architecture

GENERAL DESCRIPTION

The Z16C01/C02 CPU are members of the 16-bit processor and controller family. Designed using a RISC-like Load/Store architecture, the CPU can operate in either system or normal modes, permitting privileged operations and improving operating system organization and implementation.

To boost the main CPU's performance capability, the processor core includes hardwired control and is a 16-bit real-time processor functioning at register access speeds. Register flexibility is created by grouping or overlapping multiple registers, and by allowing extended register file capabilities as the system expands. Easy extended register file control is accomplished through a single instruction stream communication.

The CPU supports three types of interrupts (non-maskable, vectored, and non-vectored) and four traps (system call, extended process architecture instruction, privileged instructions, and segmentation trap). The vectored and non-vectored interrupts are maskable.

The processor's resources include seven data types that range from bits to 32-bit long words, and byte and word strings, plus eight user-selectable addressing modes. The nine basic instruction types can be combined with various data types and addressing modes to form a powerful set of 414 instructions.

The extended processing architecture features provide a modular approach to expanding both the hardware and software capabilities of the Z16C01/C02.

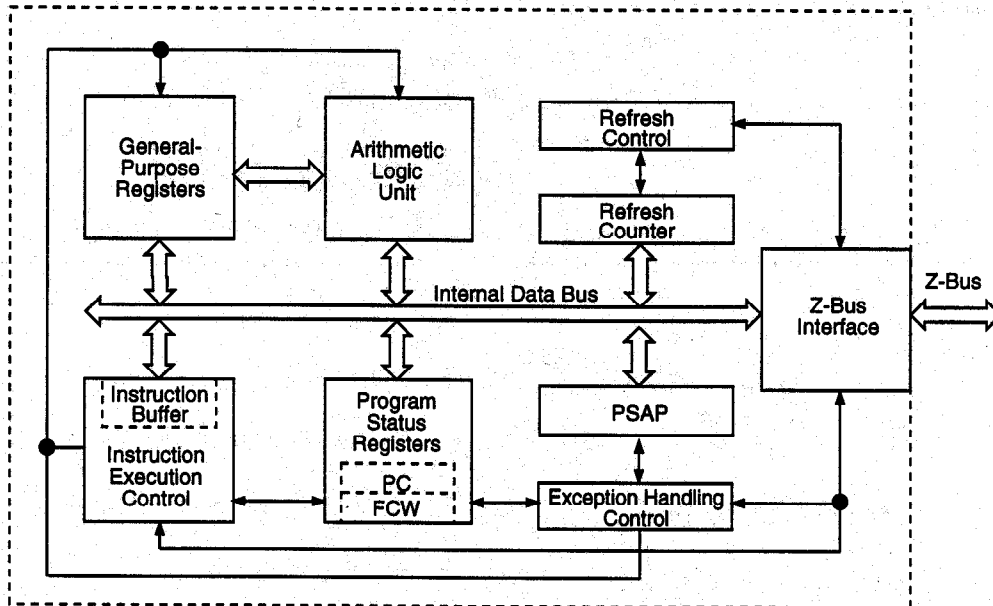
Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: /B/W (WORD is active Low); /B/W (BYTE is active Low, only).

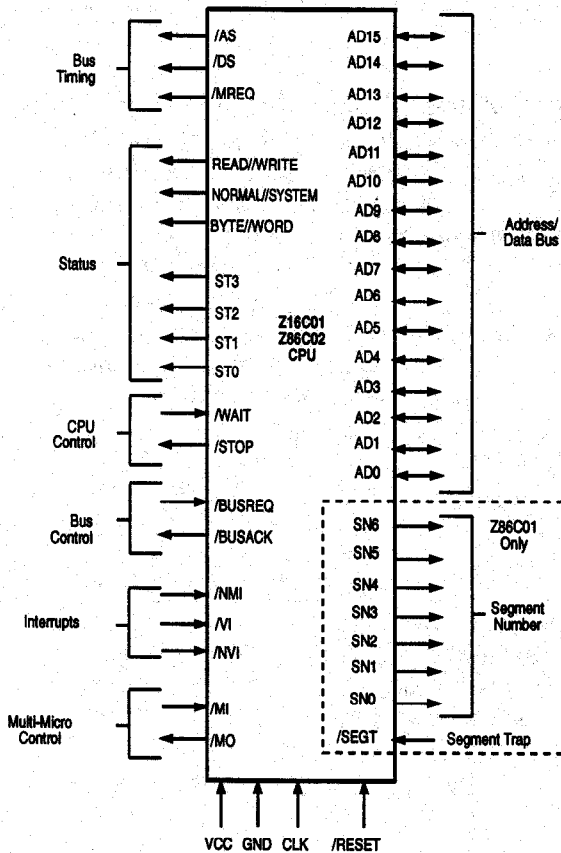
Power connections follow conventional descriptions below:

| Connection | Circuit | Device |
|--------------|-----------------|----------------------|
| Power Ground | V_{CC} GND | V_{DD} V_{SS} |

GENERAL DESCRIPTION (Continued)

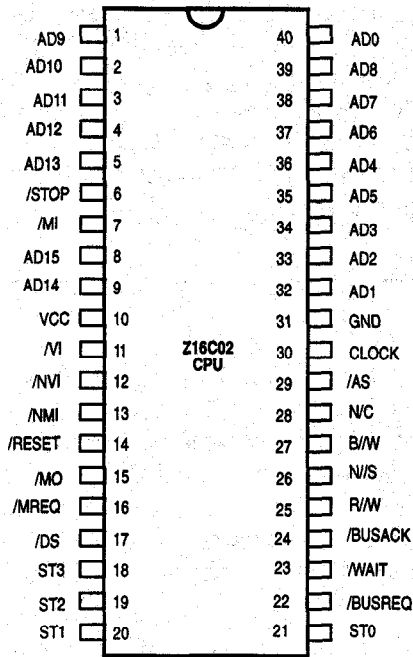


Z16C00 CPU Functional Block Diagram

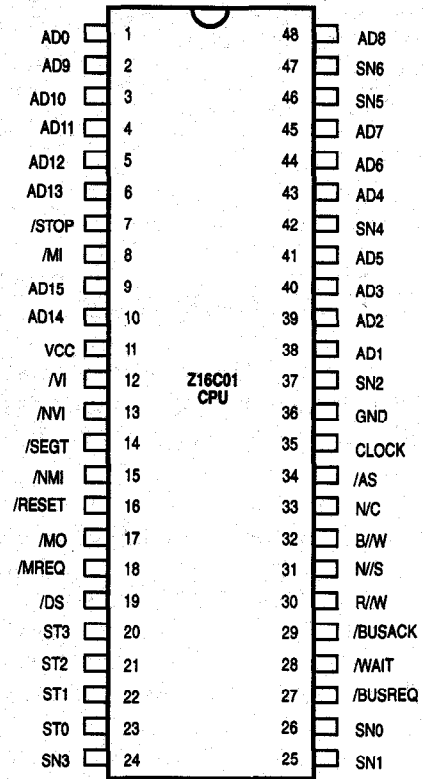


Z16C01/C02 Signal Descriptions

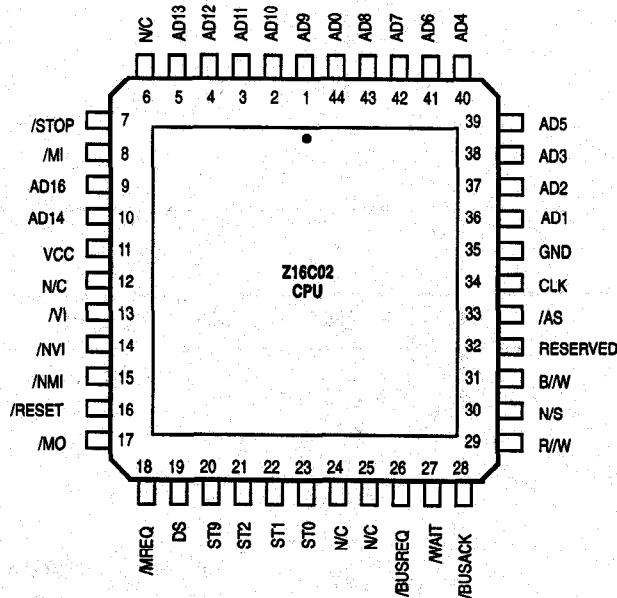
PIN DESCRIPTION



Z16C02 40-Pin PDIP



Z16C01 48-Pin PDIP



Z16C02 44-Pin PLCC

ABSOLUTE MAXIMUM RATINGS

Voltages on V_{CC} with respect to V_{SS}-0.3V to +7.0V
 Voltages on all inputs with respect to V_{SS}-0.3V to $V_{CC}+0.3V$
 Storage Temperature.....-65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operating of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

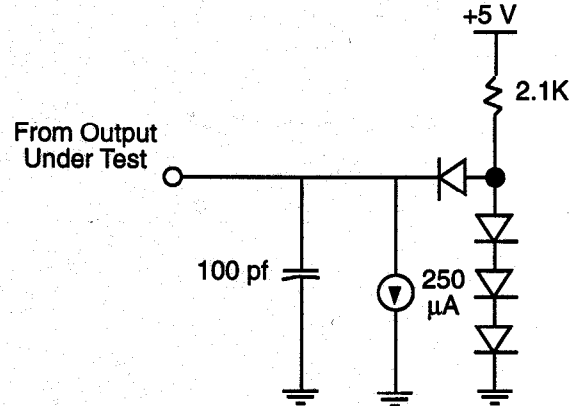
The DC characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- S = 0°C to +70°C, + 4.5V ≤ V_{CC} ≤ + 5.5V (Z16C01, Z16C02)
- E = -40°C to +100°C, + 4.5V ≤ V_{CC} ≤ + 5.5V (Z16C01, Z16C02)

All AC parameters assume a total load capacitance (including parasitic capacitances) or 100 pf max, except for parameter 6 (50 pf max). Timing reference between two output signals assume a load difference of 50 pf max.

The Ordering Information section lists package temperature ranges and product numbers.



Test Load Diagram

DC CHARACTERISTICS

| Sym | Parameter | MIN | MAX | Units | Condition |
|----------------|----------------------------------|--------------|--------------|-------|------------------------------------|
| V_{CH} | Clock Input High Voltage | $V_{CC}-0.4$ | $V_{CC}+0.3$ | V | Driven by External Clock Generator |
| V_{CL} | Clock Input Low Voltage | -0.3 | 0.45 | V | Driven by External Clock Generator |
| V_{IH} | Input High Voltage | 2.0 | $V_{CC}+0.3$ | V | |
| V_{IH} RESET | Input High Voltage on /RESET Pin | 2.4 | $V_{CC}+0.3$ | V | |
| V_{IH} NMI | Input High Voltage on NMI Pin | 2.4 | $V_{CC}+0.3$ | V | |
| V_{IL} | Input Low Voltage | -0.3 | 0.8 | V | |
| V_{OH} | Output High Voltage | 2.4 | | V | $I_{OH} = -250\mu A$ |
| V_{OL} | Output Low Voltage | | 0.4 | V | $I_{OL} = +2.0mA$ |
| I_{IL} | Input Leakage | | ±10 | μA | $0.4V \leq V_{IN} \leq +2.4V$ |
| I_{IL} SEGT | Input Leakage on /SEGT Pin | -100 | 100 | μA | |
| I_{OL} | Output Leakage | | ±10 | μA | $0.4V \leq V_{IN} \leq +2.4V$ |
| I_{CC} | V_{CC} Power Supply Current | | 35 | mA | 10MHz |

FOOTNOTES TO AC CHARACTERISTICS

| No. | Symbol | Z16C01/2 10 MHz Equation |
|-----|-----------|--------------------------------|
| 11 | TdA(DR) | 2TcC+TwCh-60ns |
| 13 | TdDS(A) | TwCl+5ns |
| 16 | TdDW(DS) | TcC+TwCh-30ns |
| 17 | TdA(MR) | TwCh-20ns |
| 19 | TwMRh | TcC-20ns |
| 20 | TdMR(A) | TwCl-20ns |
| 21 | TdDW(DSW) | TwCh-25ns |
| 22 | TdMR(DR) | 2TcC-60ns |
| 25 | TdA(AS) | TwCh-20ns |
| 27 | TdAS(DR) | 2TcC-60ns |
| 28 | TdDS(AS) | TwCl-20ns |
| 29 | TwAS | TwCh-5ns |
| 30 | TdAS(A) | TwCl-10ns |
| 32 | TdAS(DSR) | TwCl-5ns |
| 33 | TdDSR(DR) | TcC+TwCh-60ns |
| 35 | TdDS(DW) | TwCl-15ns |
| 36 | TdA(DSR) | TcC-35ns |
| 38 | TwDSR | TcC+TwCh-30ns |
| 40 | TwDSW | TcC-25ns |
| 41 | TdDSI(DR) | 2TcC-80ns |
| 43 | TwDS | 2TcC-40ns |
| 44 | TdAS(DSA) | 4TcC+TwCl-30ns |
| 46 | TdDSA(DR) | 2TcC+TwCh-75ns |
| 48 | TdS(AS) | TwCh-20ns |
| 68 | TwA | TcC-50ns |
| 69 | TdDS(s) | TwCl-10ns |

AC Timing Test Conditions:

$$V_{OL} = 0.8V$$

$$V_{OH} = 2.0V$$

$$V_{IL} = 0.8V$$

$$V_{IH} = 2.4V$$

$$V_{ILC} = 0.45V$$

$$V_{IHC} = V_{CC} - 0.4V$$

AC CHARACTERISTICS

| No. | Symbol | Parameter | Z16C01/2 10 MHz | |
|-----|-----------|--|--------------------|------|
| | | | Min | Max |
| 1 | TcC | Clock Cycle Time | 100 | ** |
| 2 | TwCh | Clock Width (High) | 40 | ** |
| 3 | TwCl | Clock Width (Low) | 40 | ** |
| 4 | TfC | Clock Fall Time | | 10 |
| 5 | TrC | Clock Rise Time | | 10 |
| 6 | TdC(SNv) | Clock+ Segment Number Valid (50pf load) | | 50 |
| 7 | TdC(SNn) | Clock +Segment Number Not Valid | 0 | |
| 8 | TdC(Bz) | Clock + Bus Float | | 50 |
| 9 | TdC(A) | Clock +Address Valid | | 50 |
| 10 | TdC(Az) | Clock + Address Float | | 50 |
| 11 | TdA(DR) | Address Valid to Read Data Required Valid | | 180* |
| 12 | TsDR(C) | Read Data to Clock Fall Setup Time | 20 | |
| 13 | TdDS(A) | /DS+Address Active | 45* | |
| 14 | TdC(DW) | Clock + Write Data Valid | | 60 |
| 15 | ThDR(DS) | Read Data to /DS Rise Hold Time | 0 | |
| 16 | TdDW(DS) | Write Data Valid to /DS Rise Delay | 110* | |
| 17 | TdA(MR) | Address Valid to /MREQ Fall Delay | 20* | |
| 18 | TdC(MR) | Clock Fall to /MREQ Fall Delay | | 50 |
| 19 | TwMRh | /MREQ Width (High) | 80* | |
| 20 | TdMR(A) | /MREQ [Address Not Active | 20* | |
| 21 | TdDW(DSW) | Write Data Valid to /DS Fall (Write) Delay | 15* | |
| 22 | TdMR(DR) | /MREQ [Read Data Required Valid | | 140* |
| 23 | TdC(MR) | Clock Fall /MREQ Rise Delay | | 50 |
| 24 | TdC(ASf) | Clock + /AS Fall Delay | | 35 |
| 25 | TdA(AS) | Address Valid to /AS Rise Delay | 20* | |
| 26 | TdC(ASr) | Clock [/AS Rise Delay | | 25 |
| 27 | TdAS(DR) | /AS + Read Data Required Valid | | 140* |
| 28 | TdDS(AS) | /DS + /AS Fall Delay | 20* | |
| 29 | TwAS | /AS Width (Low) | 35* | |
| 30 | TdAS(A) | /AS + Address Not Active Delay | 30* | |
| 31 | TdAz(DSR) | Address Float to /DS (Read) Fall Delay | 0 | |
| 32 | TdAS(DSR) | /AS + /DS (Read) Fall Delay | | 35* |
| 33 | TdDSR(DR) | /DS (Read) Fall to Read Data Required Valid | | 80* |
| 34 | TdC(DSr) | Clock Fall to /DS Rise Delay | | 30 |
| 35 | TdDS(DW) | /DS + Write Data Not Valid | 25* | |
| 36 | TdA(DSR) | Address Valid to /DS (Read) Fall Delay | 65* | |
| 37 | TdC(DSR) | Clock Rise /DS (Read) Fall Delay | | 45 |
| 38 | TwDSR | /DS (Read) Width (Low) | 110* | |
| 39 | TdC(DSW) | Clock Fall to /DS (Write) Fall Delay | | 45 |
| 40 | TwDSW | /DS (Write) Width (Low) | 75* | |
| 41 | TdDSI(DR) | /DS (I/O) [Read Data Required Valid | | 120* |
| 42 | TdC(DSf) | Clock [/DS (I/O) Fall Delay | | 45 |
| 43 | TwDS | /DS (I/O) Width (Low) | 160* | |
| 44 | TdAS(DSA) | /AS + /DS (Acknowledge) Fall Delay | 410* | |
| 45 | TdC(DSA) | Clock + /DS (Acknowledge) Fall Delay | | 45 |
| 46 | TdDSA(DR) | /DS (Acknowledge) [Read Data Required Delay | | 165* |
| 47 | TdC(S) | Clock Rise to Status Valid Delay | | 50 |

AC CHARACTERISTICS (Continued)

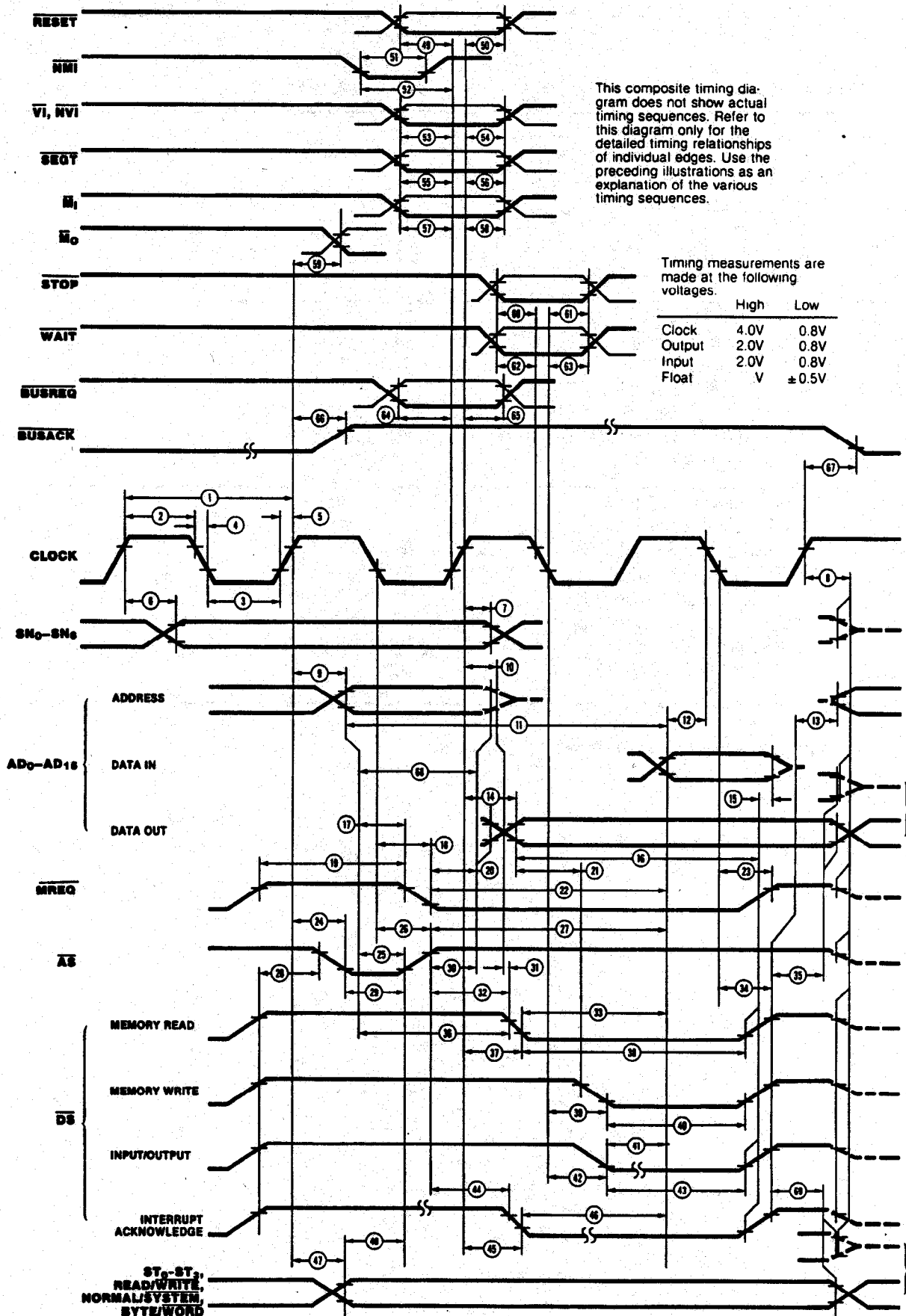
| No. | Symbol | Parameter | Z16C01/2 | |
|-----|-----------|------------------------------------|---------------|-----|
| | | | 10 MHz Min | Max |
| 48 | TdS(AS) | Status Valid to /AS Rise Delay | 20* | |
| 49 | TsR(C) | /RESET to Clock Rise Setup Time | 35 | |
| 50 | ThR(C) | /RESET to Clock Rise Hold Time | 0 | |
| 51 | TwNMI | /NMI Width (Low) | 35 | |
| 52 | TsNMI(C) | /NMI to Clock Rise Setup Time | 35 | |
| 53 | TsVI(C) | /VI, /NVI to Clock Rise Setup Time | 35 | |
| 54 | ThVI(C) | /VI, /NVI to Clock Rise Hold Time | 10 | |
| 55 | TsSGT(C) | /SEGT to Clock Rise Setup Time | 35 | |
| 56 | ThSGT(C) | /SEGT to Clock Rise Hold Time | 10 | |
| 57 | TsMI(C) | /MI to Clock Rise Setup Time | 35 | |
| 58 | ThMI(C) | /MI to Clock Rise Hold Time | 0 | |
| 59 | TdC(MO) | Clock Rise to /MO Delay | | 50 |
| 60 | TsSTP(C) | /STOP to Clock Fall Setup Time | 35 | |
| 61 | ThSTP(C) | /STOP to Clock Fall Hold Time | 0 | |
| 62 | TsW(C) | /WAIT to Clock Fall Setup Time | 20 | |
| 63 | ThW(C) | /WAIT to Clock Fall Hold Time | 5 | |
| 64 | TsBRQ(C) | /BUSREQ to Clock Rise Setup Time | 35 | |
| 65 | ThBRQ(C) | /BUSREQ to Clock Rise Hold Time | 5 | |
| 66 | TdC(BAKr) | Clock Rise to /BUSACK Rise Delay | | 35 |
| 67 | TdC(BAKf) | Clock Rise to /BUSACK Fall Delay | | 35 |
| 68 | TwA | Address Valid Width | 50* | |
| 69 | TdDS(S) | /DS Rise to STATUS Not Valid | 30* | |

* Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.

** Clock may be stopped.

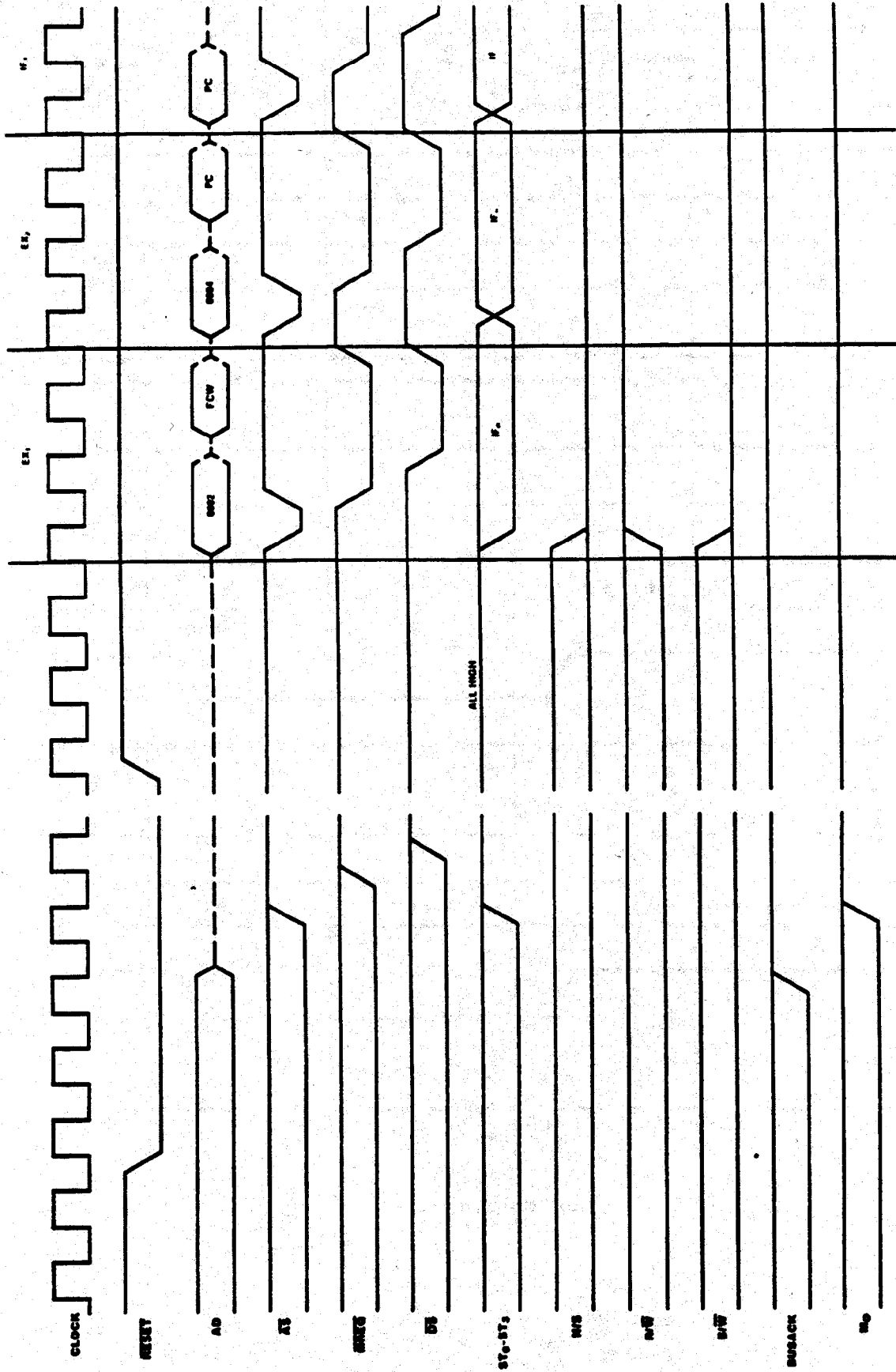
† Units in nanoseconds (ns).

COMPOSITE AC TIMING DIAGRAM



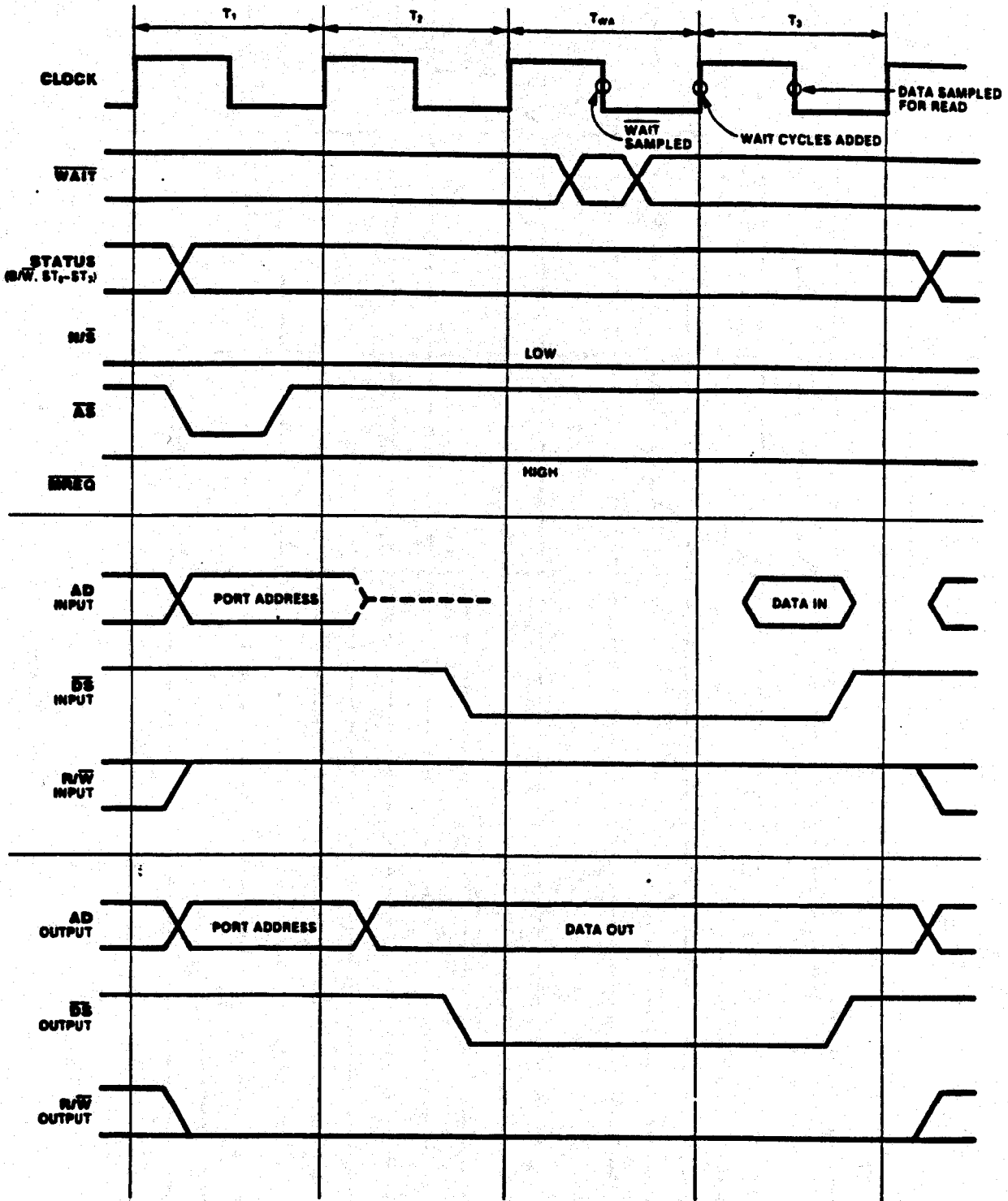
Composite AC Timing

TIMING DIAGRAMS



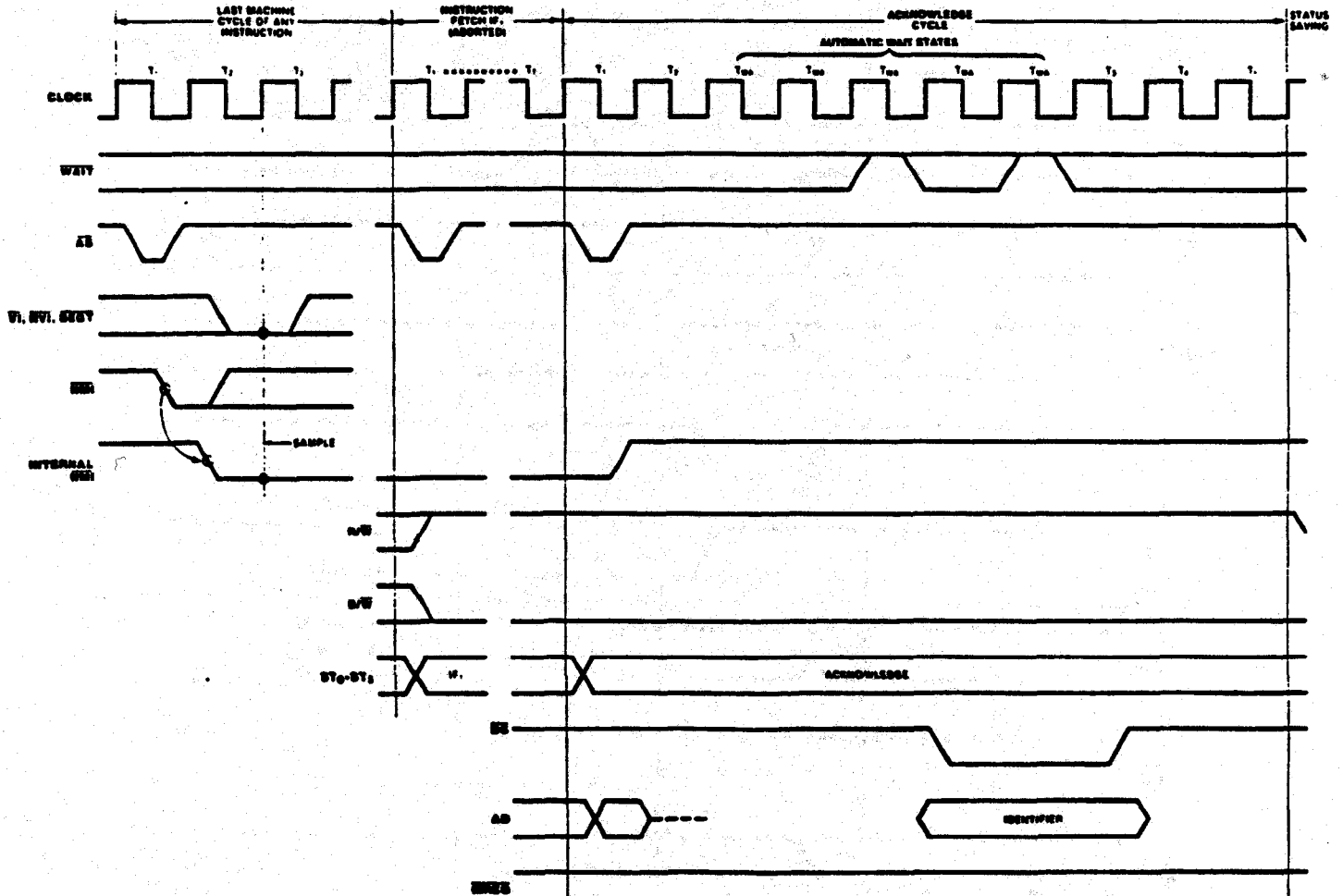
Reset Timing

TIMING DIAGRAMS (Continued)



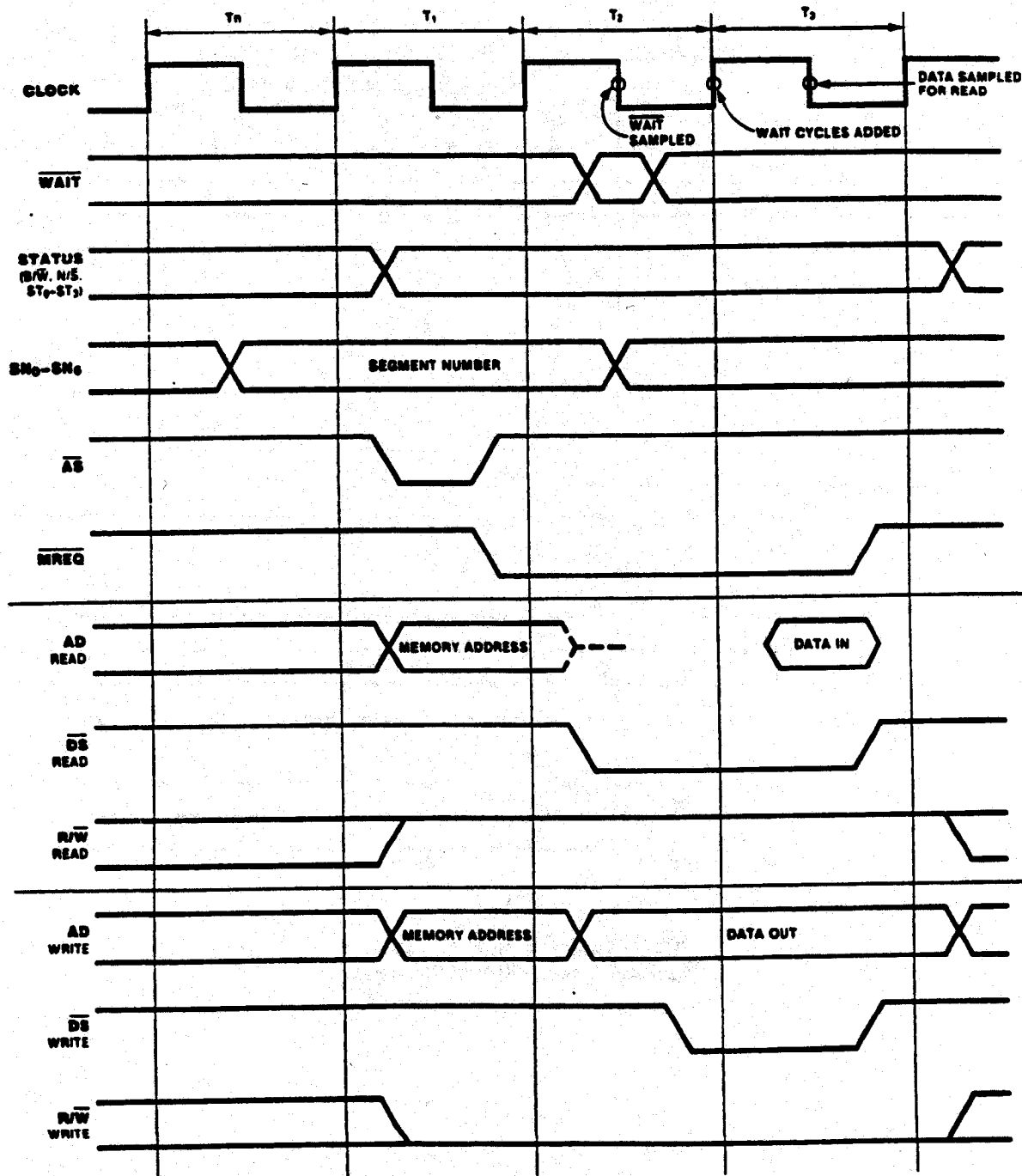
Input/Output Timing

TIMING DIAGRAMS (Continued)



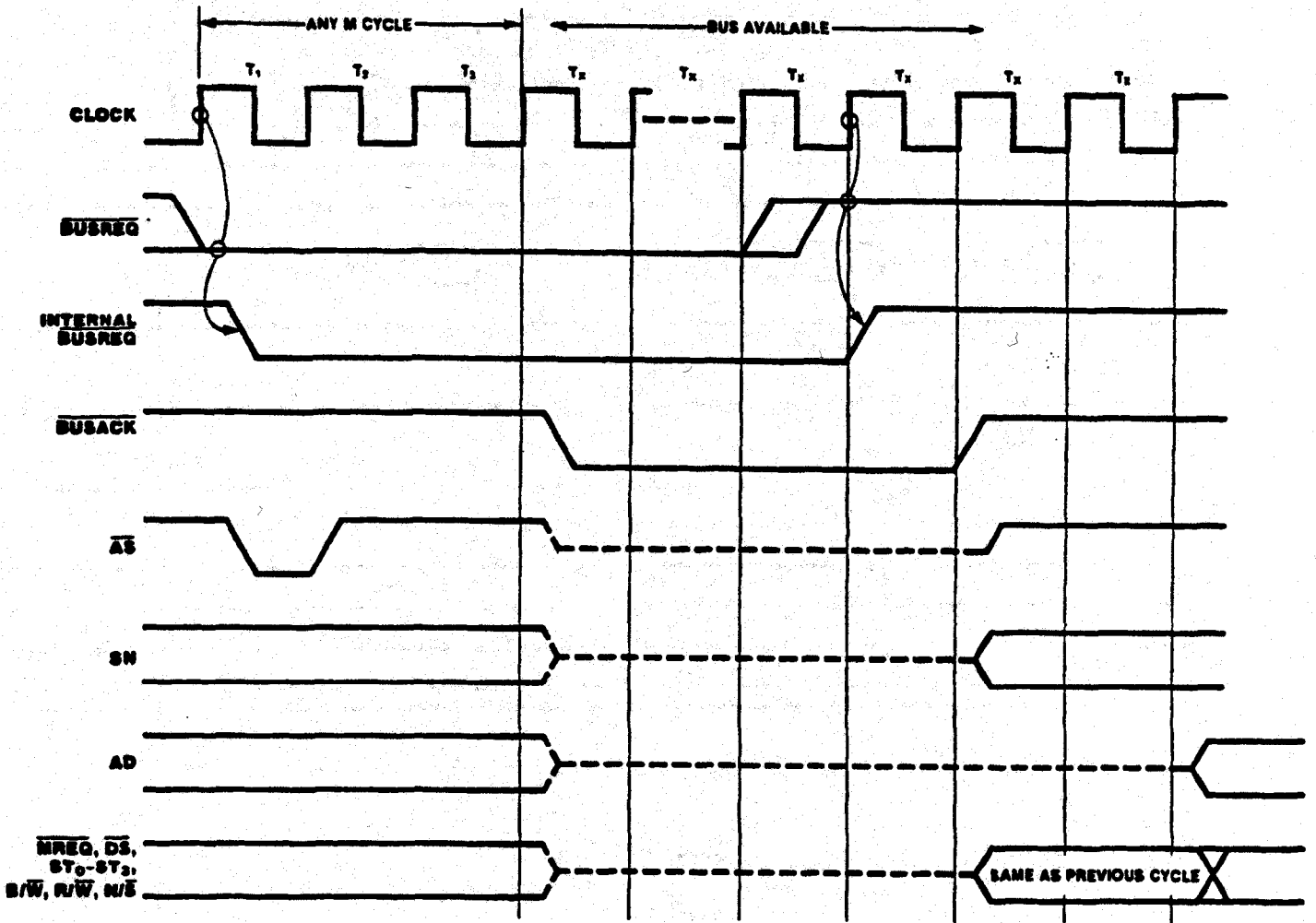
Interrupt and Segment Trap
Request/Acknowledge Timing

TIMING DIAGRAMS (Continued)



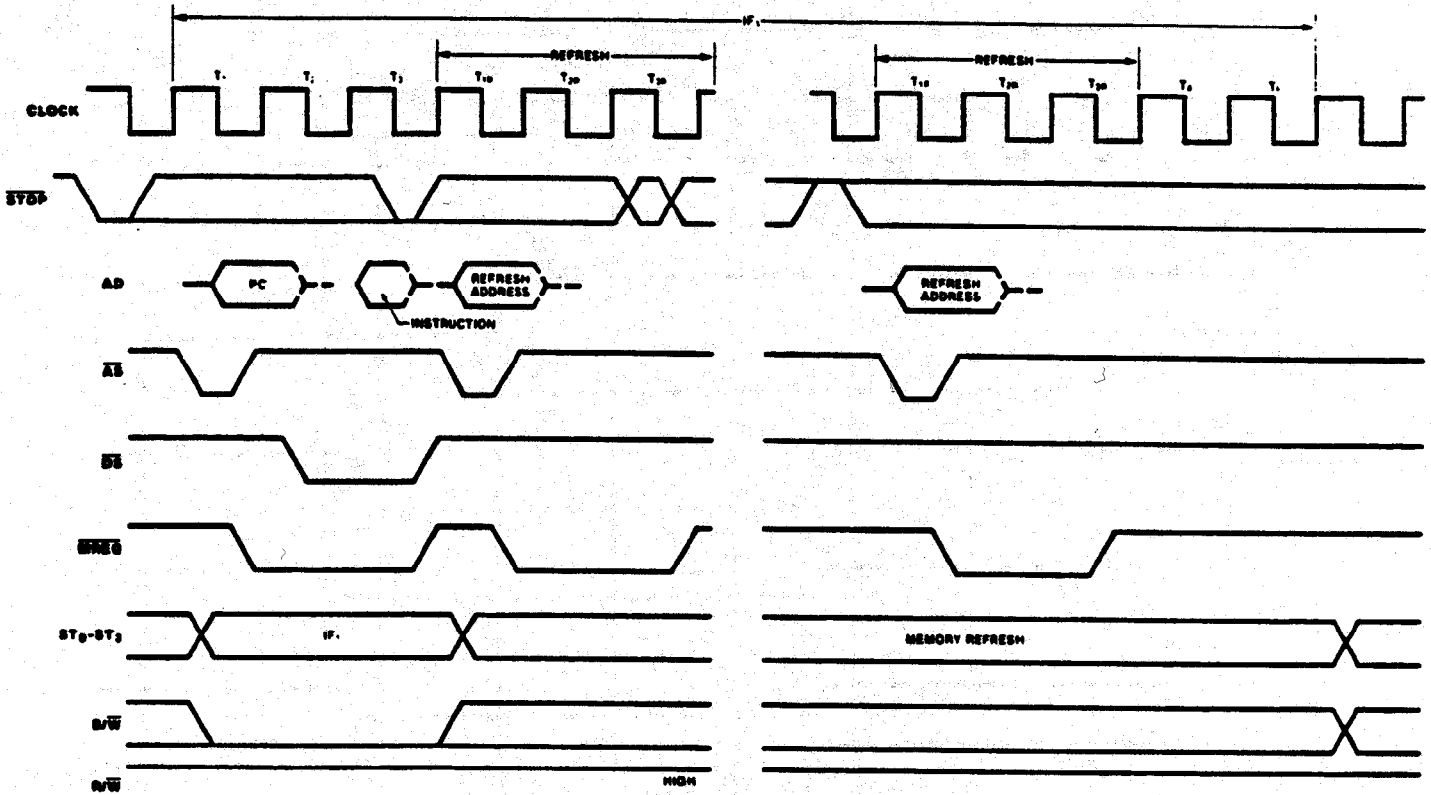
Memory Read and Write Timing

TIMING DIAGRAMS (Continued)



Bus Request/Acknowledge Timing

TIMING DIAGRAMS (Continued)



Stop Timing

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